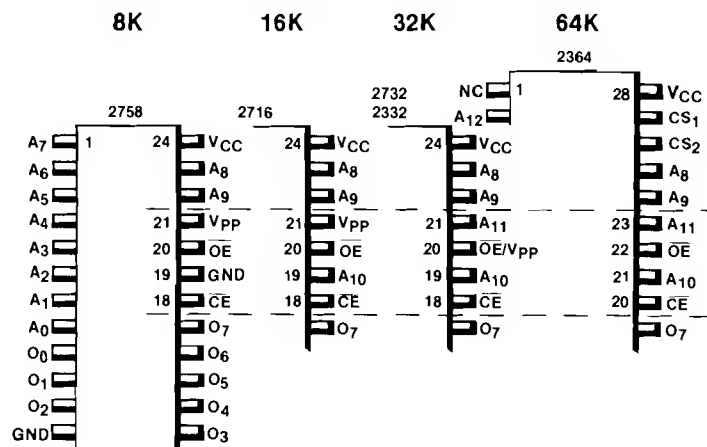




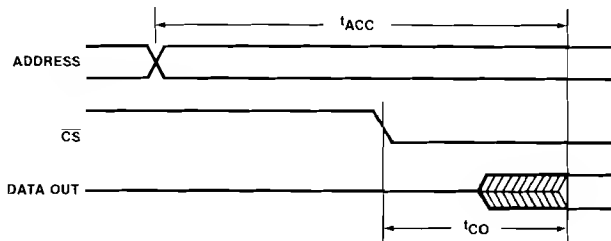
intel®

EPROM/ROM Compatibility

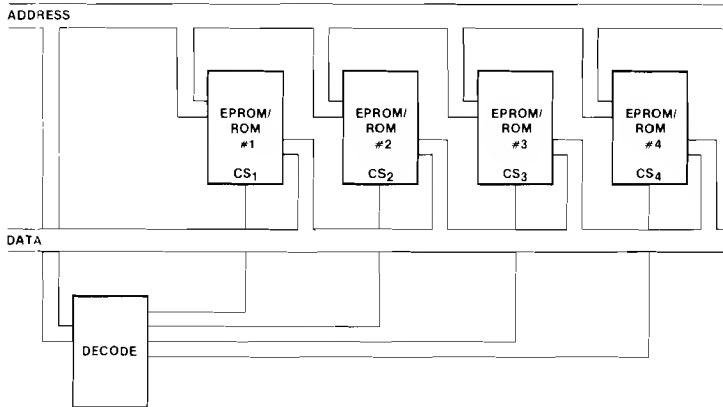
EPROM/ROM COMPATIBLE FAMILY



- Everything's the same except for 4 pins.
- This presentation discusses the techniques required to utilize any member of this family in the same DIP site.
- Note that the 2758/2716 nomenclature has been changed to reflect actual function usage.

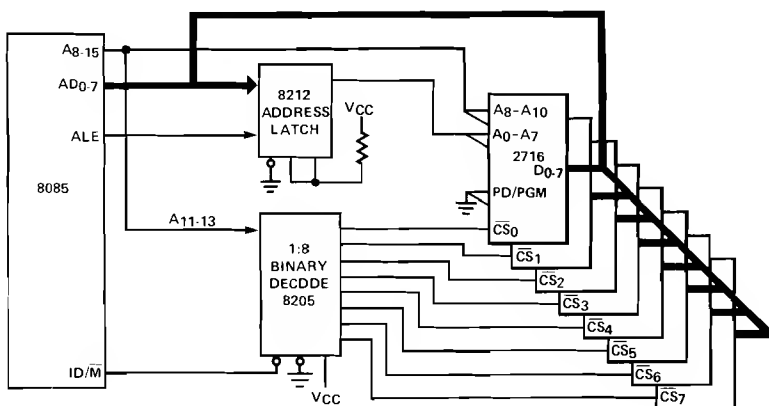


- Traditional decode scheme utilizes time difference between t_{ACC} and t_{CO} to allow time for decode function.

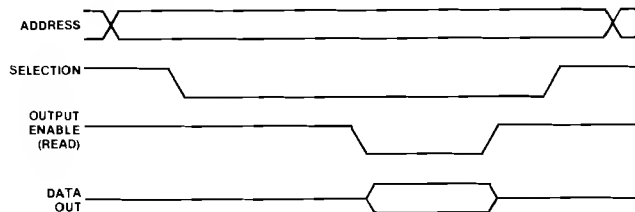


- Inadvertant address changes can cause multiple device selection.
- Most microprocessors have some states where addresses are undefined: If this occurs during memory cycle, bus contention results.

TRADITIONAL 16K EPROM SYSTEM

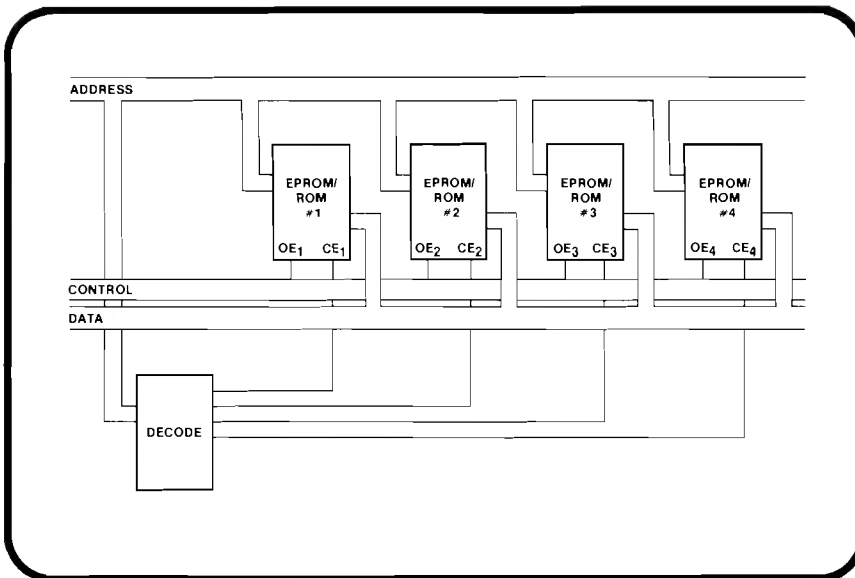


- Actual system showing traditional decode implementation.
- Traditional scheme is not compatible with new high performance microprocessors.
- A new decode scheme is required.
- Note that PD/PGM is connected to GND and CS is used to control selection.

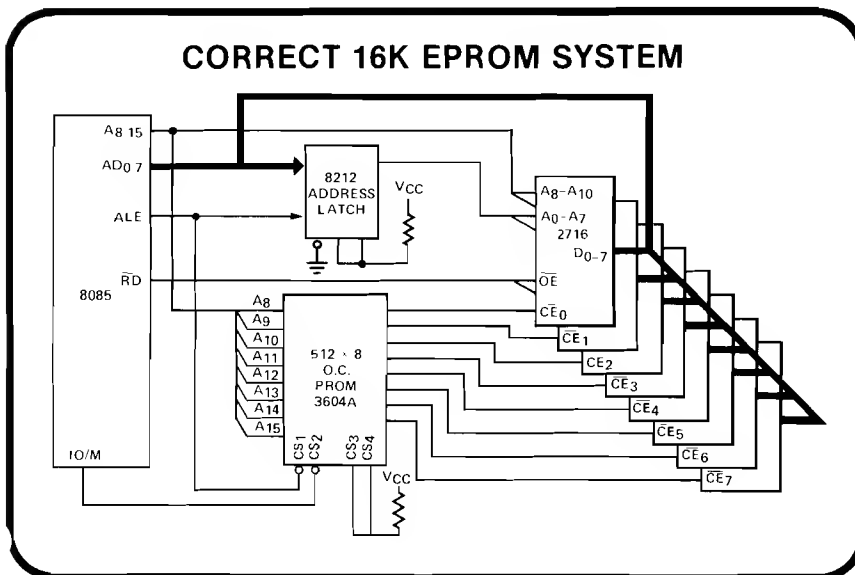


- New decode scheme requires separation of device selection and output control (OE).
- Address bus used as before to accomplish device selection.
- Memory device outputs enabled only when required.

- Control function now completely independent from device selection process.



- Actual system showing new decode scheme.
- Note that the 2716 has not changed, only the function names for Pin 18 and Pin 20.
- All future references to the 2716 will reflect this new nomenclature. Pin 18 is now \overline{CE} , Pin 20 is now \overline{OE} .
- This scheme accomplished by using \overline{CE} (PD) as the primary decode. \overline{OE} (CS) is now controlled by previously unused signal. RD now controls data on and off the bus by way of \overline{OE} .
- A selected 2716 is available for systems which require \overline{CE} access of less than 450 ns for decode network operation.
- The use of a PROM as a decoder allows for:
 - ALE is required for Edge Enabled devices (32K and 64K), and is optional for 2716.
 - Compatibility with upward (and downward) memory expansion.
 - Easy assignment of ROM memory modules, compatible with PL/M modular software concepts.

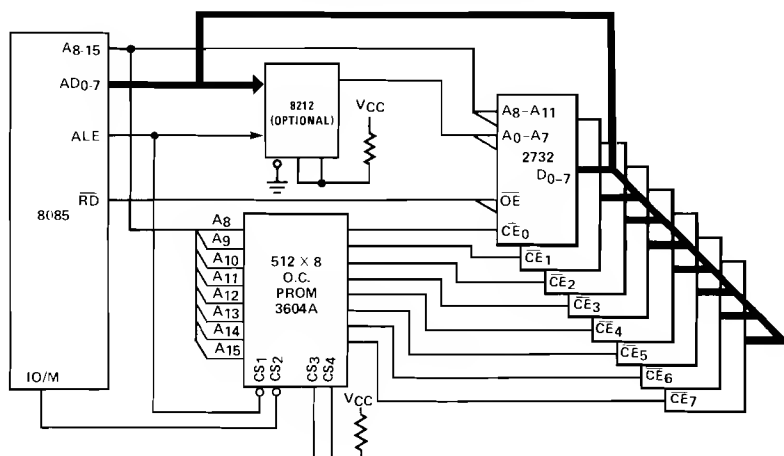


SYSTEM UPGRADE TO 32K EPROM/ROM

	2716	2332/2732	
PIN 21	V _{PP} (V _{CC})	A ₁₁	COMMON MEMORY ARRAY CONNECTION
PIN 20	\overline{OE}	\overline{OE}	NO CHANGE
PIN 19	A ₁₀	A ₁₀	NO CHANGE
PIN 18	\overline{CE}	CE	AUTOMATIC POWER DOWN
8212	REQUIRED	OPTIONAL	EDGE ENABLED DEVICES HAVE ON CHIP LATCHES

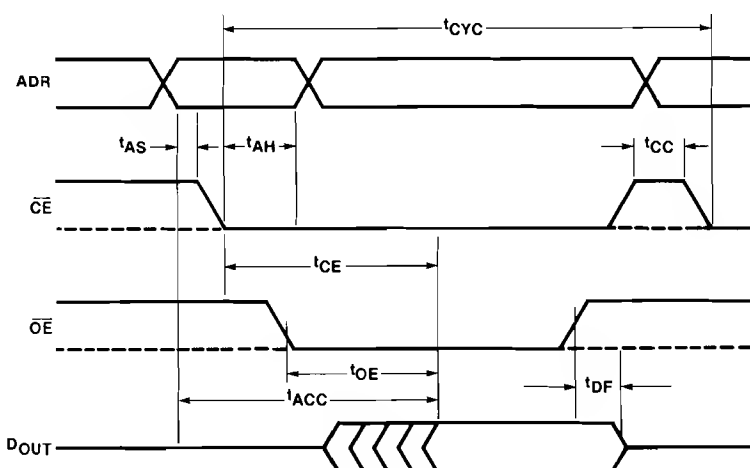
- 2732/2332 are plug-in replacements for 2716.
- One board level jumper on Pin 21 required to select either V_{PP} (V_{CC}) or A₁₁.
- Pins 18, 19 and 20 have maintained same function as on 2716.
- Note that V_{PP} is equal to V_{CC} for read (not programming) function of 2716.

32K EPROM SYSTEM



- Connections the same as for 16K EPROM.
- By planning ahead, ALE was used as condition for decode, thus assuring that t_{CC} time requirement will be met.

EDGE ENABLED PRODUCT WAVEFORMS



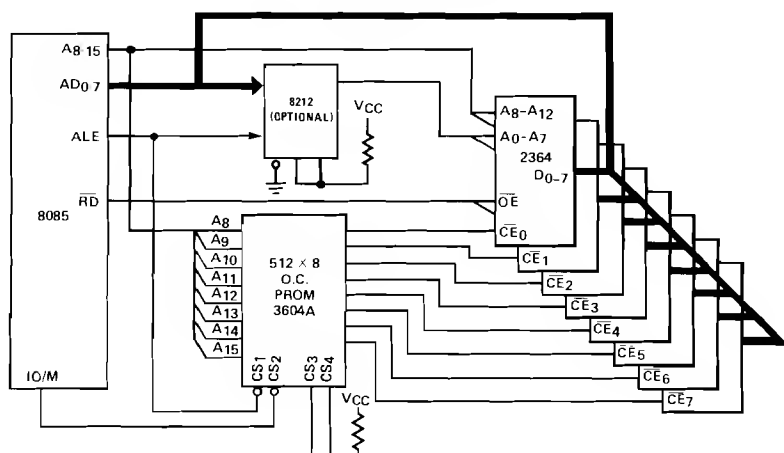
- New Intel ROMs/EPROMs use Edge Enabled concept.
- Cycle time does not equal access time.
- Internally, Edge Enabled devices have completely static arrays with some clocked peripheral circuits.
- CE may remain high or low indefinitely — however, it must be high a minimum of 100 ns (t_{CC}) prior to a high to low edge transition.

SYSTEM UPGRADE TO 64K ROM

2332/2732	2364	
24-PIN	28-PIN	PLUG-IN — NO JUMPERS
		LOWER 24 PINS ARE IDENTICAL
V _{CC}	CS ₂	CODE THIS CS ₂ ACTIVE HIGH

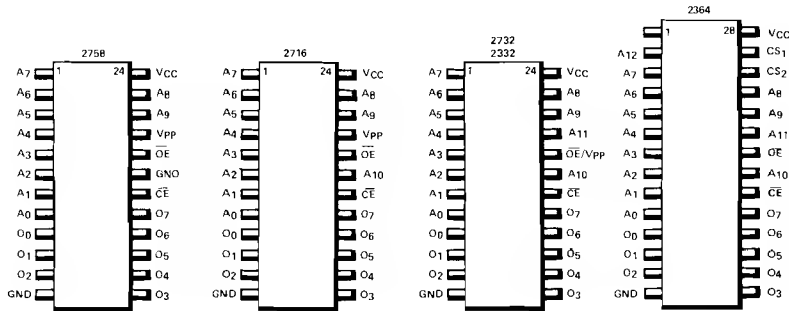
- Remember to code CS₂ active high.
- Board can be laid out for 28-pin device initially and thereby allow total flexibility from 8K through 64K.

64K ROM SYSTEM

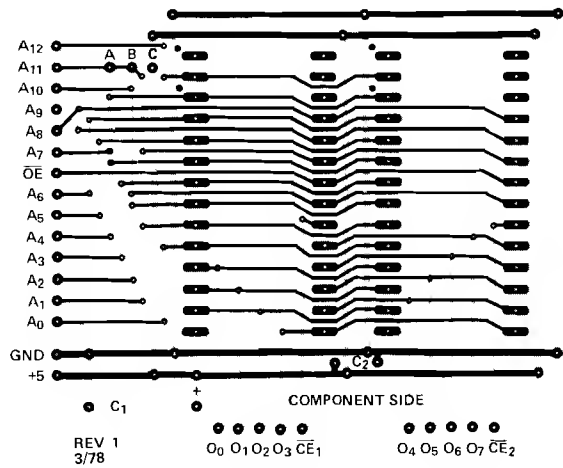


- As with 32K and 16K, all connections are the same at the system level, only the EPROM/-ROM changes.
- As in the 32K system, the 8212 address latch is optional for Edge Enabled devices.

EPROM/ROM COMPATIBLE FAMILY



- The entire family.
- By laying out a PC board now for 28 pin sites, and allowing for jumper selection at A₁₁, modularity from 1K byte through 8K bytes can be achieved, on the same card, with either ROM or EPROM.



- Example of printed circuit layout to accomodate entire compatible family.
- Provision for A₁₁/V_{CC} jumper on pin 21 shown at A, B and C.